# Lab 1 Structural Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? **\_\_\_**

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: **\_\_\_\_**

Student Name: Wonhee Lee  
Student ID: 54872959  
Date Completed: 04-18-2020  
Time Spent: Reviewing Digital Design Material: 30min   
 Design/Preparation Work: 1h  
 VHDL Coding & Debugging: 4h

## Structural Overview

Replace this text w/ the % you feel you completed the lab. Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

## Lab 1 NAND Equation

F3’F2’ + F3’F1’F0’ //Conversion rules

= ((F3’F2’)’(((F1’F3’)’)’F0’)’)’

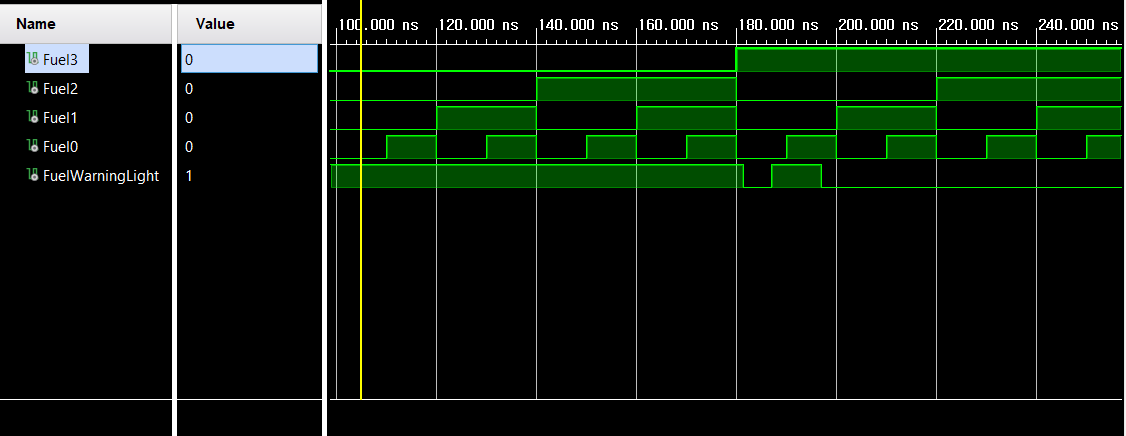
## Lab 1 Circuit and Input-to-Output Delay

Provide a drawing/figure/circuit of your final structural equation in terms of gates here. You can use Visio or other gate drawing software here or attach a picture of your circuit as long as it is legible.



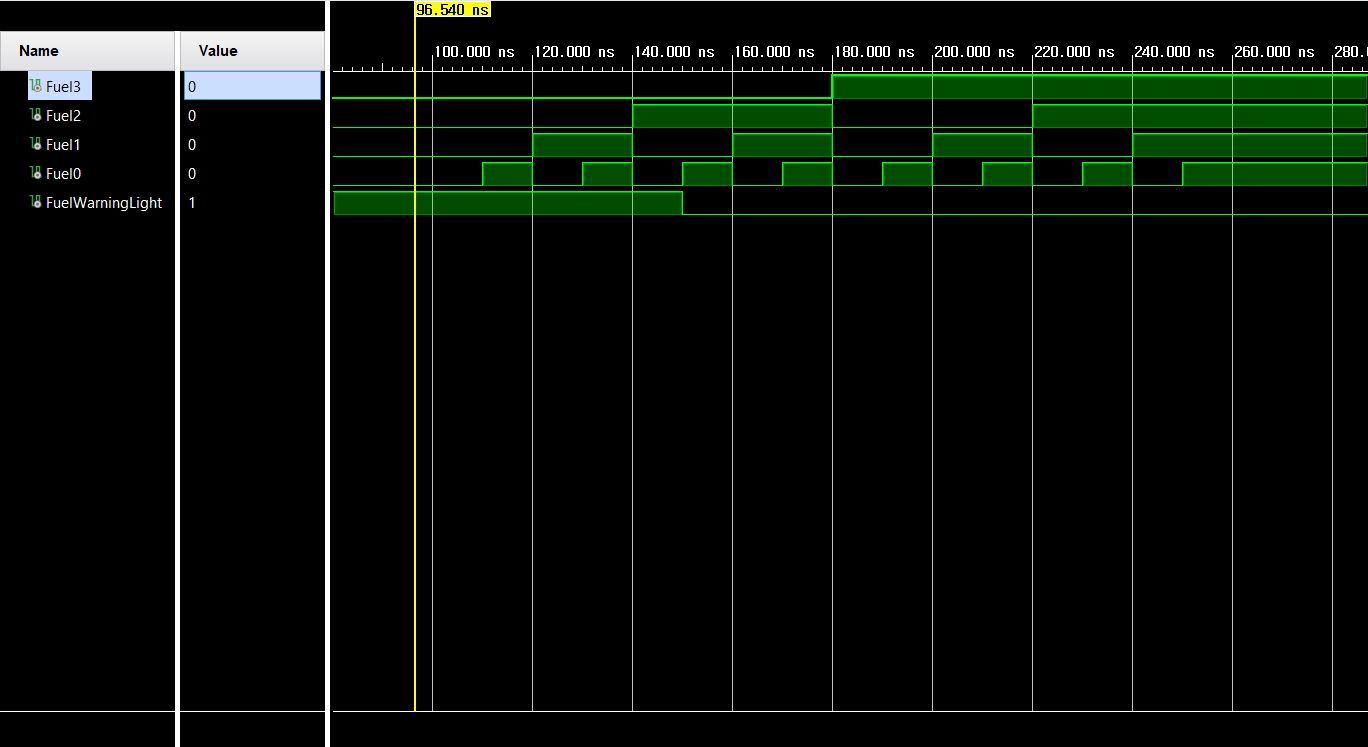
Delay of circuit: 7 ns

## Lab 1 Structural Simulation Graph



## Lab 1 Structural and Behavioral Simulation Graph Comparisons

Behavioral



Due to the structure of NAND gate, FuelWarningLight changed to 1 for a few ns when it wasn’t expected. Then it goes to 0 as it should be.